

REMARKS

Claims 1-3 are pending in this application. It is gratefully acknowledged that the Examiner has found allowable subject matter in Claim 3.

In the Office Action, the Examiner has rejected independent Claim 1 under 35 U.S.C. §102(e) as allegedly being anticipated by *Butler et al.* (U.S. Patent No. 6,333,939 B1), and independent Claim 2 under 35 U.S.C. §103(a) as allegedly being unpatentable over *Butler* in view of *Challa et al.* (U.S. Patent No. 6,453,181 B1). More specifically, in both rejections, the Examiner cites *Butler* (column 3, lines 22-31) as teaching *calculating the difference of edge timings between a main clock and a low frequency clock*, as is recited in both Claims 1 and 2. This cited section of *Butler* reads as follows:

In one embodiment, the synchronization logic circuit comprises at least one digital latch for aligning a rising edge of the low frequency clock signal to a rising edge of the high frequency clock signal. The frequency error estimator may also comprise a counter for counting a number of high frequency clock signal periods per low frequency clock signal period; and an accumulator for accumulating a difference between an expected number of high frequency clock signal periods per low frequency clock signal period and an actual number of high frequency clock signal periods per low frequency clock signal period.

In the above section, it is respectfully submitted that there is no disclosure of calculating the difference of edge timings between a main clock and a low frequency clock. Instead, *Butler* appears to teach counting a difference between a number of high frequency clock signal periods per low frequency clock signal period.

Further, Claims 1 and 2 recite *comparing the calculated timing difference with a predetermined difference reference value*. Again, the Examiner cites *Butler* (column 3, lines 28-31) as teaching this recitation. However, this section of *Butler* teaches an accumulator for accumulating a

difference between (1) an expected number of high frequency clock signal periods per low frequency clock signal period, and (2) an actual number of high frequency clock signal periods per low frequency clock signal period. It is respectfully submitted that this is not an equivalent of comparing the calculated timing difference with a predetermined difference reference value, as is recited in Claims 1 and 2. Further, it is respectfully submitted that *Challa* does not cure these deficiencies. Therefore, it is respectfully submitted that the Examiner is incorrect in rejecting Claims 1 and 2, and it is respectfully requested that the rejections of Claims 1 and 2 are withdrawn.

As independent Claim 2 is believed to be in condition for allowance, dependent Claim 3 will also be in condition for allowance as being dependent upon independent Claim 2.

Accordingly, all of the claims pending in the Application, namely, Claims 1-3, are believed to be in condition for allowance. Should the Examiner have any questions, he is requested to contact the undersigned at the number indicated below. Early and favorable consideration of the claims is respectfully requested.

Respectfully submitted,



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